

Master's Thesis

FPGA Acceleration of String Search Techniques in Huge Data Sets

Searching strings in huge data sets, e.g., in search engines and bioinformatics, relies on suitable data structures that exhibit low storage requirements and allow for efficient operations, such as construction, insertion, indexing, and ranking. Important examples for such data structures are based on the Burrows Wheeler Transformation (BWT) or the Indexed Reversible Transformation (IRT). This project will investigate ways to accelerate operations on these data structures by customized hardware and present a hardware accelerator implemented on a Field-Programmable Gate Array (FPGA).

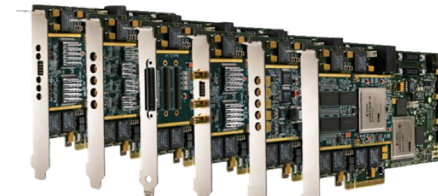
Type of project

- Study existing techniques (BWT, IRT) and acceleration approaches
- Design and implement an FPGA accelerator exploiting different levels of parallelism
- Compare to software reference, evaluate scalability

Prerequisites

- Good programming skills
- Knowledge of BWT / IRT or FPGAs / hardware design is beneficial

<u>B</u> ANANA	BWT →	0	ABANA	N
A <u>N</u> ANAB		1	ANABA	N
N <u>A</u> NABA		2	ANANA	B
A <u>N</u> ABAN		3	B ANANA	A
N <u>A</u> BANA		4	NABANA	A
A <u>B</u> ANAN		5	NANABA	A



Contact and Supervisors

Prof. Dr. Marco Platzner, O3.207
platzner@uni-paderborn.de

Prof. Dr. Stefan Böttcher, F2.217
stb@uni-paderborn.de

