FPGA Overlays with RapidWright

Bachelor/Master Thesis

**In a Nutshell**
- Get familiar with new open source tool RapidWright
- Identify design aspects to use RapidWright for FPGA overlays
- Implement overlay design
- Demonstrate usage with different applications and/or overlays

FPGAs can accelerate a wide range of applications in terms of performance and energy efficiency by customizing the hardware to the required compute and data access patterns. However, FPGAs are traditionally difficult to program and require time-consuming synthesis processes (conceptually similar to software compilation). The synthesis processes can run for hours or days from start to finish and need to be repeated for every change in the application.

Both challenges can be met with overlay architectures, which provide an abstraction layer on top of the original FPGA fabric. Structurally programmable overlays exhibit operators and connections for entire data words instead of individual bits, whereas soft processors can be programmed by instructions using ordinary compilers. But how can we efficiently design customizable overlays?

In early 2018, a new open source tool called RapidWright has been released. RapidWright can read and write so-called Design CheckPoint (DCP) files during the design synthesis to speed-up the processes and reuse results for later/similar use cases (see Figure, right side). This gives a new exciting research direction for FPGA overlays: pre-synthesized modules (already synthesized and placed and routed out-of-context DCP files) can be used as smaller building blocks for a programmable FPGA overlay. The modules can be of different size and functionality or they can be replicated or relocated depending on the use case. In the simplified application in the figure, the add-module could be replaced by another module (for example a mul-module).

**Recommended Skills**
- Interest in hardware acceleration and computer architecture (mainly FPGAs)
- Interest/Experience in hardware programming

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